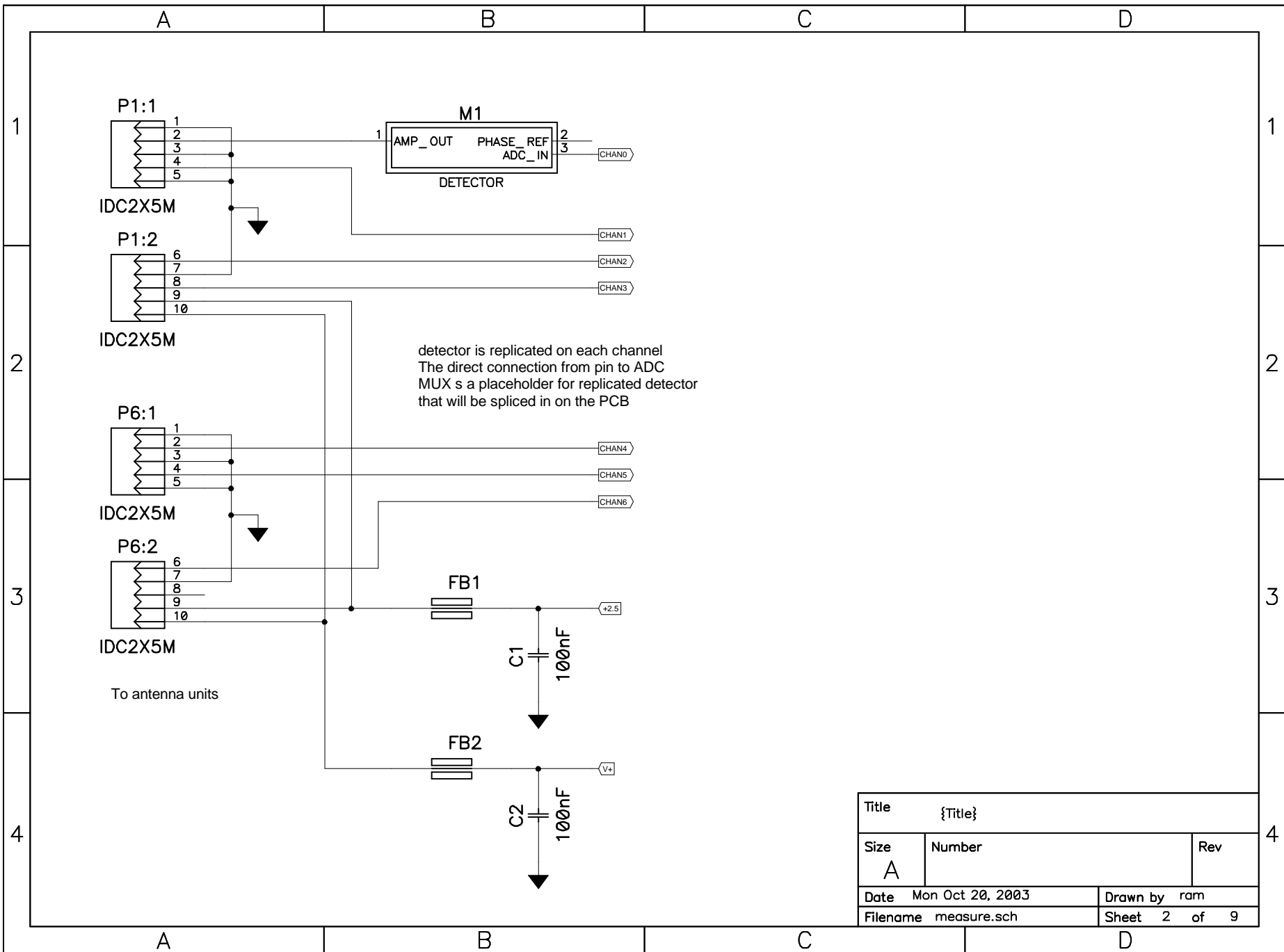
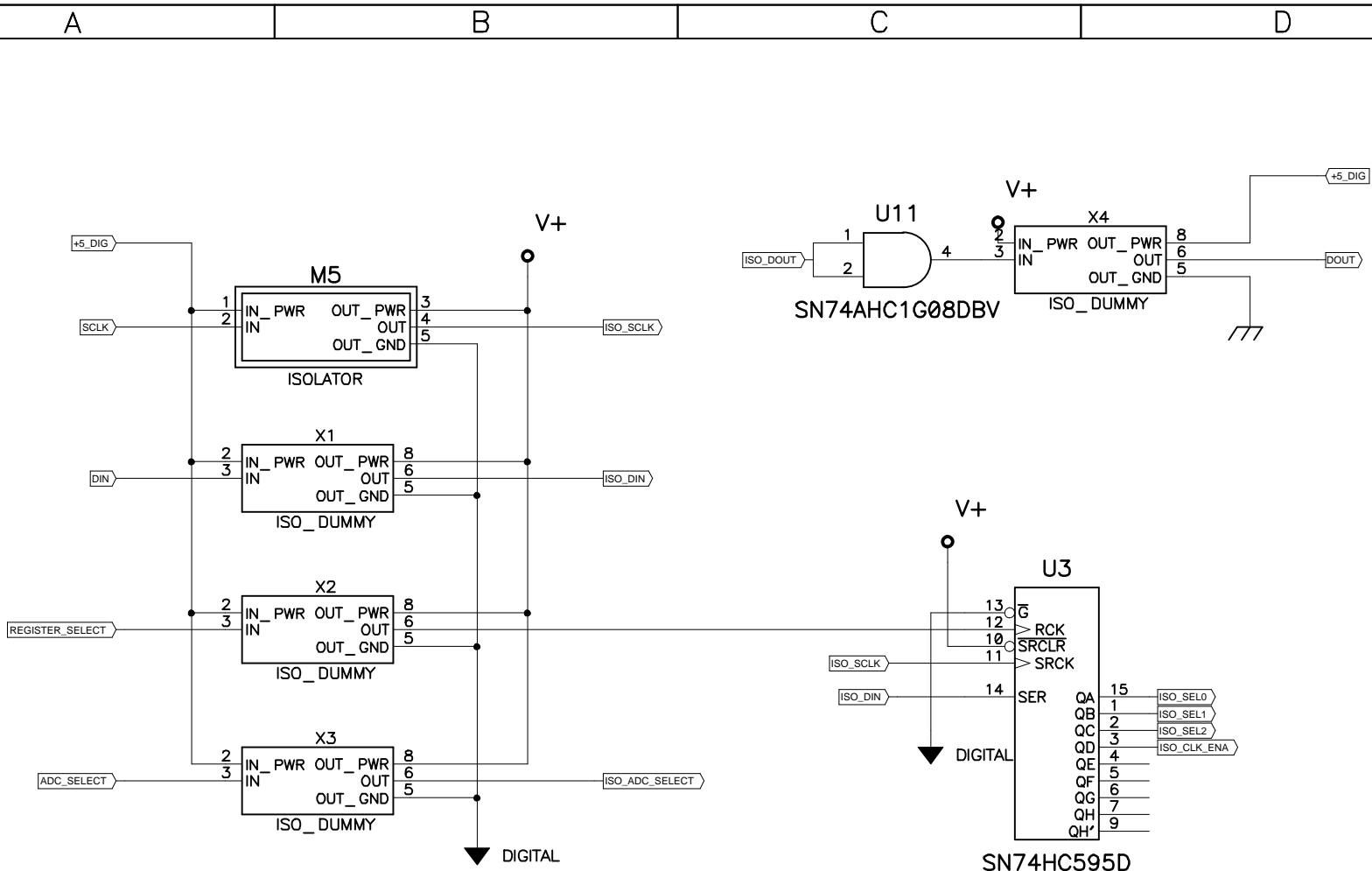


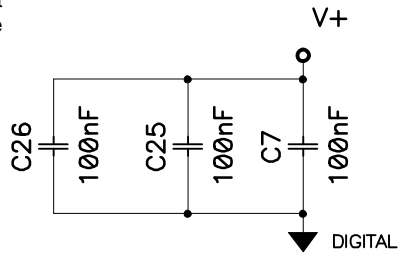
Title {Title}		
Size A	Number	Rev
Date Mon Oct 20, 2003	Drawn by ram	
Filename measure.sch	Sheet 1 of 9	



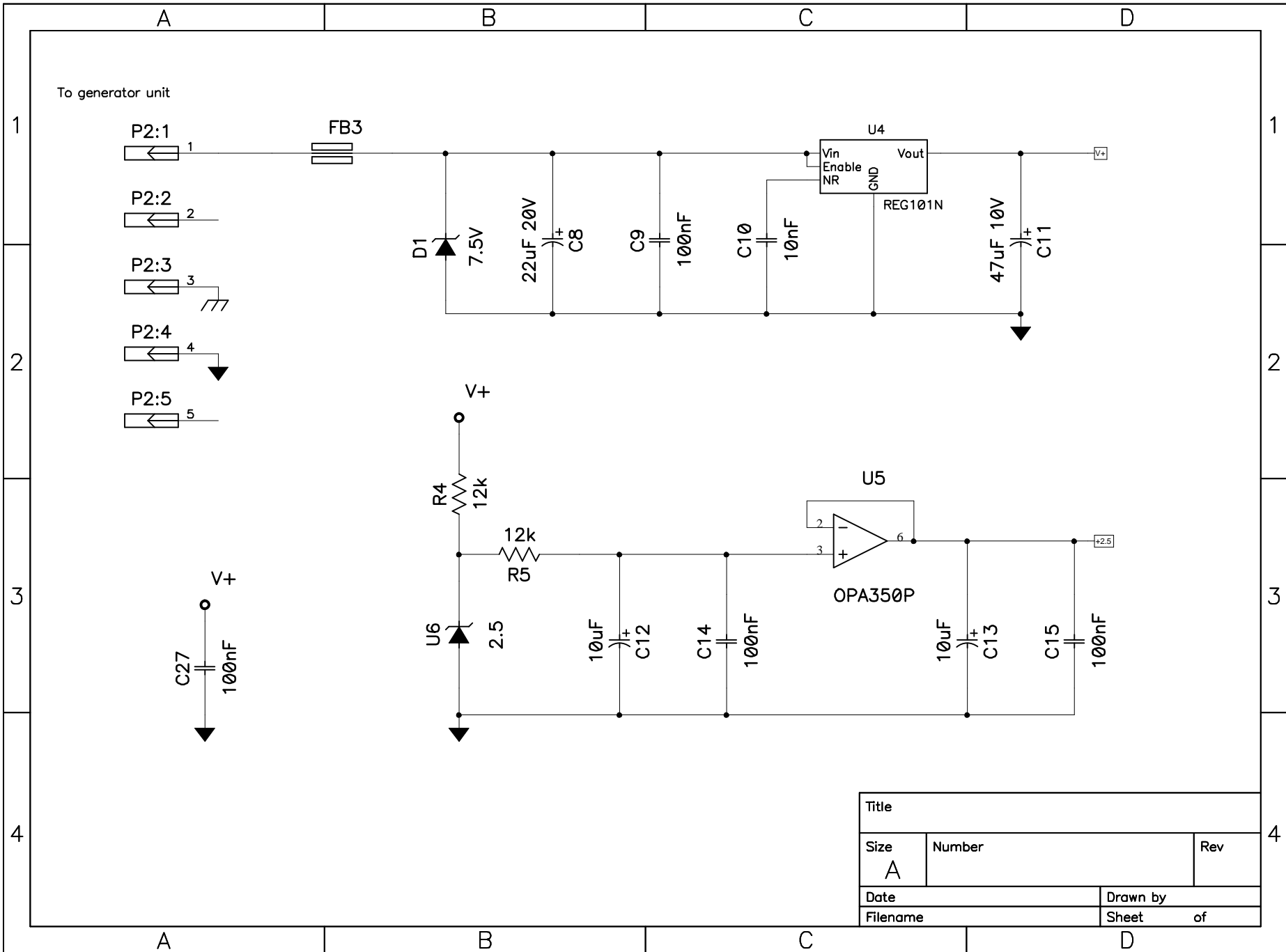
Title		{Title}
Size	Number	Rev
A		
Date	Mon Oct 20, 2003	Drawn by ram
Filename	measure.sch	Sheet 2 of 9



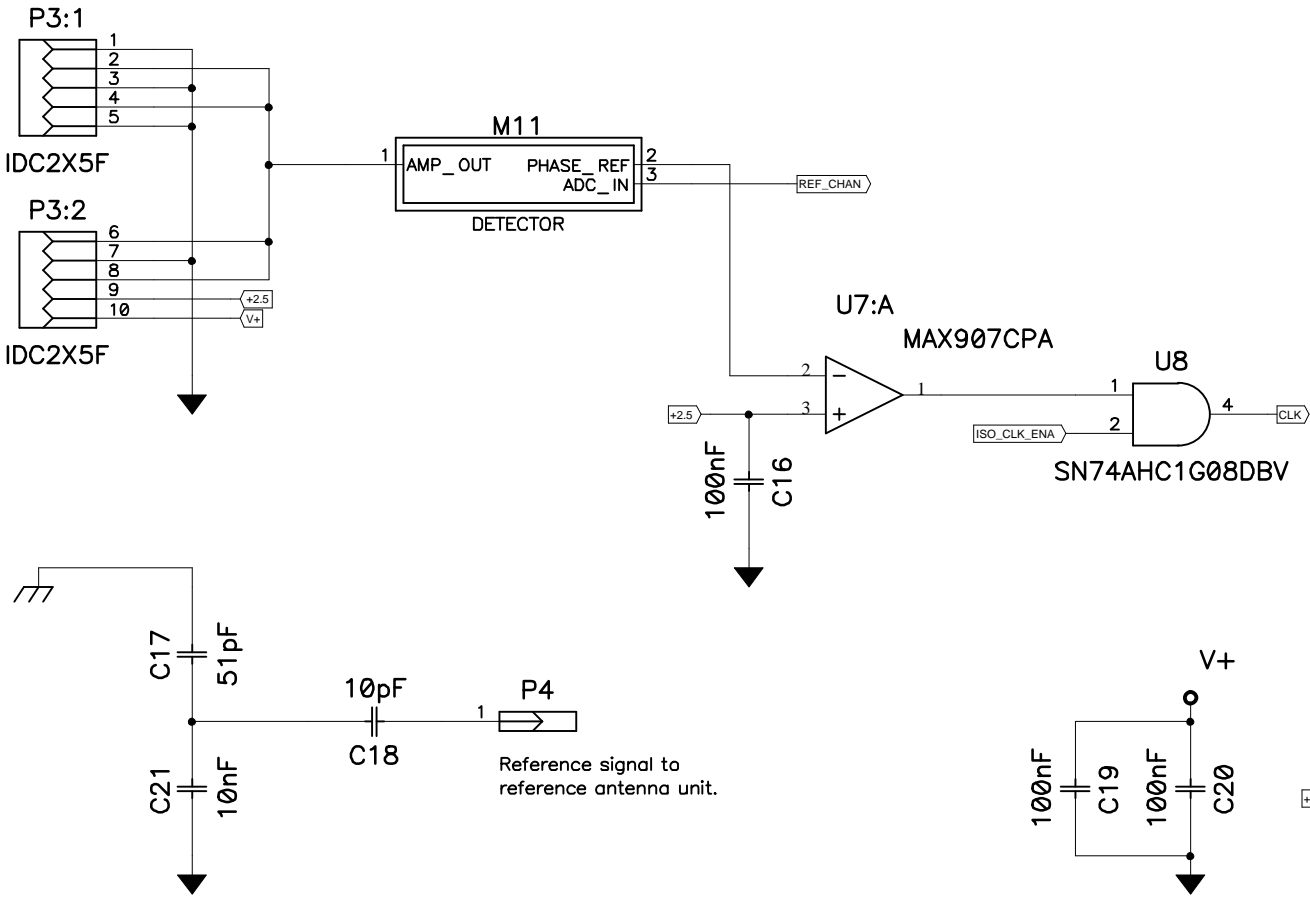
ISO_DUMMY is a dummy component that will be replaced with a copy of the isolator layout in the PCB.



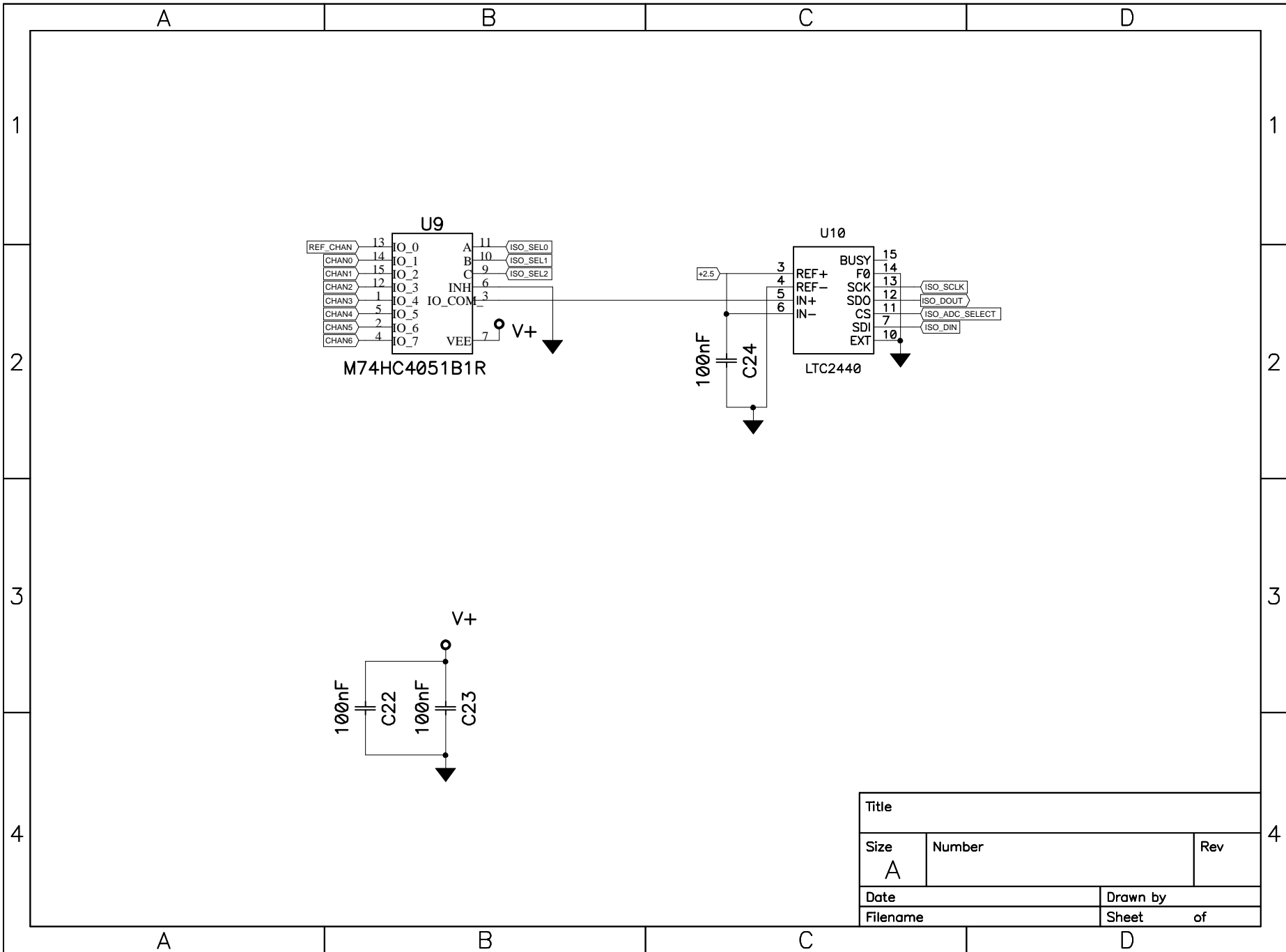
Title		
Size	Number	Rev
A		
Date		Drawn by
Filename		Sheet of



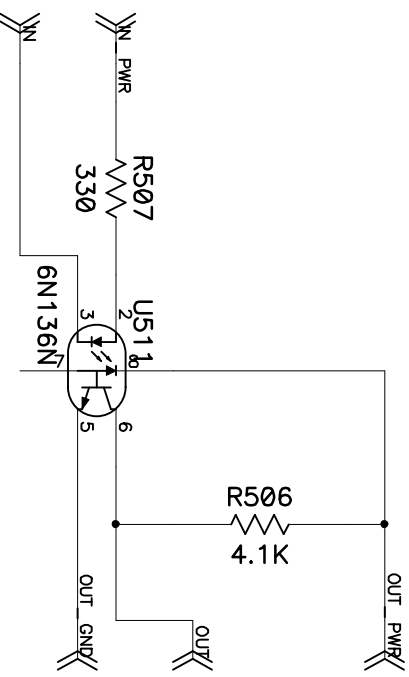
Input from reference antenna unit.



Title		
Size A	Number	Rev
Date	Drawn by	
Filename	Sheet	of



Title		
Size A	Number	Rev
Date	Drawn by	
Filename	Sheet of	



Title		
Size	Number	Rev
A		
Date	Drawn by	
Filename	Sheet	of
	D	

A

B

C

D

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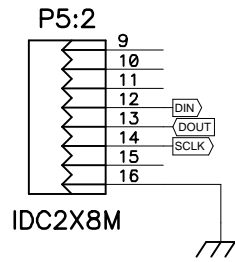
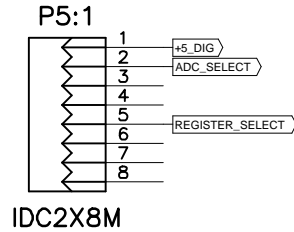
3

3

4

4

To P1, PORTSD&E
on ATMEGA128 dev board



Title		
Size A	Number	Rev
Date		Drawn by
Filename		Sheet of

A

B

C

D

A

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2

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4

Power Table				
Ref Des	Device(Type)	Package	V+	GNDA
U3	SN74HC595D	SO16	16	8
U5	OPA350P	DIP-8	7	4
U7	MAX907CPA	DIP-8	8	4
U8	SN74AHC1G08DBV	SO-GS/P.95_BB	5	3
U9	M74HC4051B1R	DIP-16	16	8
U10	LTC2440	SSO-G16/D5	2	1,8,9,16
U11	SN74AHC1G08DBV	SO-GS/P.95_BB	5	3
U102	OPA2336P	DIP-8	8	4

Title

Size Number

A

Rev

Date

Filename

Drawn by

Sheet

of

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